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DATE: September 9, 2004

TO: Office of Initial Patent Examination (703) 308-1202
(ADDRESSEE) (EXTENSION)

USPTO (703) 746-9195
(LOCATION) (FAX NUMBER)

FROM: Pat Thomas for Joanna Chlu (512) 996-6839
(SENDER) (EXTENSION)

TOTAL NUMBER OF PAGES 10 (Including this page)

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Docket No.: SC12888TH
Applicant: William C. Moyer et al.
Serial No.: 10/631,136
Art Unit: 2186
Filed: July 31, 2003

ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:

1.	x	1 page Facsimile Cover Sheet
2.	x	1 page Request for Correction of Filing Receipt
3.	x	1 page Copy of Filing Receipt Showing Changes Requested
4.	x	1 page Copy of Fee Transmittal Submitted with Application
5.	x	1 page Copy of Claims as Submitted with Application

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ON: 9-9-04
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
William C. Moyer et al.

Serial No.: 10/631,136

Filed: July 31, 2003

For: PREFETCH CONTROL IN A DATA
PROCESSING SYSTEM

) Examiner: Unassigned
)
) Group Art Unit: 2186
)
) Docket No.: SC12888TH
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OFFICE OF INITIAL PATENT EXAMINATION
COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313-1450

REQUEST FOR CORRECTION OF FILING RECEIPT

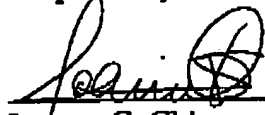
Applicants respectfully request correction of two errors on the USPTO Filing Receipt. In particular, through no fault of the Applicants, the number of total claims and the number of individual claims are incorrect. Applicants have provided a copy of the claims and the fee transmittal which were included with the original filing papers. Applicants respectfully request that total claims be changed to 23 and individual claims to 3.

A copy of the first page of the USPTO Filing Receipt showing the desired corrections is submitted with the present request.

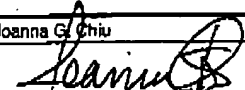
Respectfully submitted,

9/8/04

Date



Joanna G. Chiu
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Registration No. 43,629
Telephone No.: (512) 996-6849
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FEE TRANSMITTAL		Complete Known																																																																																																																																																						
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<input type="checkbox"/> Check <input type="checkbox"/> Credit card <input type="checkbox"/> Money Order <input type="checkbox"/> Other <input type="checkbox"/> None <input checked="" type="checkbox"/> Deposit Account Deposit Account Number 502117 Deposit Account Name Motorola, Inc. The Director is authorized to: (check all that apply) <input checked="" type="checkbox"/> Charge fee(s) indicated below <input checked="" type="checkbox"/> Credit any overpayments <input type="checkbox"/> Charge any additional fee(s) during the pendency of this application <input type="checkbox"/> Charge fees(s) indicated below, except for the filing fee to the above-identified deposit account.		3. ADDITIONAL FEES <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="2">Large Entity</th> <th colspan="2">Small Entity</th> <th rowspan="2">Fee Description</th> </tr> <tr> <th>Code</th> <th>Fee (\$)</th> <th>Code</th> <th>Fee (\$)</th> </tr> </thead> <tbody> <tr><td>1051</td><td>130</td><td>2051</td><td>65</td><td>Surcharge - late filing fee or oath</td></tr> <tr><td>1052</td><td>50</td><td>2052</td><td>25</td><td>Surcharge - late Provisional filing</td></tr> <tr><td>1053</td><td>130</td><td>1053</td><td>130</td><td>Non-English specification</td></tr> <tr><td>1812</td><td>2520</td><td>1812</td><td>2520</td><td>For filing a request for expedited Reexamination</td></tr> <tr><td>1804</td><td>920*</td><td>1804</td><td>920*</td><td>Requesting publication of SIR prior to Examiner action</td></tr> <tr><td>1806</td><td>1040*</td><td>1805</td><td>1840*</td><td>Requesting publication of SIR after Examiner action</td></tr> <tr><td>1251</td><td>110</td><td>2251</td><td>55</td><td>Extension for reply within first month</td></tr> <tr><td>1252</td><td>410</td><td>2252</td><td>205</td><td>Extension for reply within second month</td></tr> <tr><td>1253</td><td>930</td><td>2253</td><td>485</td><td>Extension for reply within third month</td></tr> <tr><td>1254</td><td>1480</td><td>2254</td><td>725</td><td>Extension for reply within fourth month</td></tr> <tr><td>1255</td><td>1970</td><td>2255</td><td>985</td><td>Extension for reply within fifth month</td></tr> <tr><td>1401</td><td>320</td><td>2401</td><td>160</td><td>Notice of Appeal</td></tr> <tr><td>1402</td><td>320</td><td>2402</td><td>160</td><td>Filing a brief in support of an appeal</td></tr> <tr><td>1403</td><td>280</td><td>2403</td><td>140</td><td>Request for oral hearing</td></tr> <tr><td>1451</td><td>1510</td><td>1451</td><td>1510</td><td>Petition to institute a public use proceeding</td></tr> <tr><td>1452</td><td>110</td><td>2452</td><td>55</td><td>Petition to revive - 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Name (Print/Type) Joanna G. Chiu		Registration No. 43,629 Telephone (512)996-6839																																																																																																																																																						
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CLAIMS

1. A data processing system, comprising:

a first master;

5 storage circuitry, coupled to the first master, for use by the first master;

a first control storage circuit which stores a first prefetch limit;

a prefetch buffer; and

10 prefetch circuitry, coupled to the first control storage circuit, to the prefetch buffer, and to the storage circuitry, said prefetch circuitry selectively prefetches a predetermined number of lines from the storage circuitry into the prefetch buffer, wherein the first prefetch limit controls how many prefetches occur between misses in the prefetch buffer.

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2. The data processing system of claim 1, further comprising:

a first prefetch counter, wherein the prefetch circuitry selectively prefetches the predetermined number of lines from the storage circuitry into the prefetch buffer based on the first prefetch counter.

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3. The data processing system of claim 1, further comprising:

a second master, wherein the storage circuitry is coupled to the second master and is for use by the second master; and

25 a second control storage circuit which corresponds to the second master and stores a second prefetch limit.

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4. The data processing system of claim 3, wherein the first prefetch limit controls how many prefetches for the first master occur between misses in the prefetch buffer on read requests from the first master, and wherein the second prefetch limit controls how many prefetches for the second master occur between misses in the prefetch buffer on read requests from the second master.
5. The data processing system of claim 3, further comprising:
- a first prefetch counter, wherein the prefetch circuitry selectively prefetches the predetermined number of lines for the first master from the storage circuitry into the prefetch buffer based on the first prefetch counter; and
 - a second prefetch counter, wherein the prefetch circuitry selectively prefetches a predetermined number of lines for the second master from the storage circuitry into the prefetch buffer based on the second prefetch counter.
6. The data processing system of claim 3, wherein the prefetch circuitry:
- selectively prefetches the predetermined number of lines for the first master based on the first prefetch counter in response to at least one of a hit or a miss in the prefetch buffer corresponding to an access request from the first master; and
 - selectively prefetches the predetermined number of lines for the second master based on the second prefetch counter in response to at least one of a hit or a miss in the prefetch

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buffer corresponding to an access request from the second master.

7. The data processing system of claim 1, wherein the prefetch
5 circuitry selectively prefetches the predetermined number of lines
in response to at least one of a hit or a miss in the prefetch buffer.
8. The data processing system of claim 1, wherein the first control
storage circuit is programmable.
- 10
9. The data processing system of claim 1, further comprising a request
monitor coupled to the first control storage circuitry, wherein the
request monitor selectively updates the prefetch limit based on a
number of buffer hits in the prefetch buffer accessed between two
15 misses in the prefetch buffer.
10. A method for performing prefetch in a data processing system,
comprising:
receiving a plurality of access requests from a master to access
20 storage circuitry; and
using a prefetch limit to limit a number of prefetches performed
between misses in a prefetch buffer resulting from at least a
portion of the plurality of access requests.
- 25 11. The method of claim 10, further comprising providing a prefetch
control circuit to store the prefetch limit.

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12. The method of claim 10, wherein using the prefetch limit to limit the number of prefetches comprises:
counting prefetches after a miss in the prefetch buffer to determine when the prefetch limit is reached.

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13. The method of claim 12, wherein each prefetch prefetches a single line from the storage circuitry.

14. The method of claim 13, wherein each single line prefetch is performed in response to at least one of a hit or a miss in the prefetch buffer.

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15. A method for performing prefetch in a data processing system, comprising:

15

receiving a read request from a master to access storage circuitry;

determining whether the read request results in a hit or a miss in a prefetch buffer;

if the read request results in a hit, selectively performing a

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prefetch of a predetermined number of lines from the storage circuitry into the prefetch buffer based at least in part on a prefetch counter reaching a first value; and

if the read request results in a miss, performing a demand fetch in response to the read request and setting the prefetch counter to a second value.

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16. The method of claim 15, wherein selectively performing the prefetch of the predetermined number of lines is further based on

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whether or not the predetermined number of lines is already present in the prefetch buffer.

17. The method of claim 16, further comprising:

5 prefetching the predetermined number of lines from the storage circuitry and updating the prefetch counter when the read request results in a hit, the prefetch counter has not reached the first value, and the predetermined number of lines is not already present in the prefetch buffer.

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18. The method of claim 17, wherein the second value corresponds to a prefetch limit and wherein updating the counter comprises decrementing the prefetch counter.

15 19. The method of claim 17, wherein the first value corresponds to a prefetch limit and wherein updating the counter comprises incrementing the prefetch counter.

20. The method of claim 16, further comprising:

20 not prefetching from the storage circuitry when the read request results in a hit and the prefetch counter has reached the first value.

21. The method of claim 15, further comprising prefetching a

25 predetermined number of lines from the storage circuitry when the read request results in a miss.

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22. The method of claim 15, wherein selectively performing a prefetch
of a predetermined number of lines from the storage circuitry into
the prefetch buffer based at least in part on a prefetch counter
reaching a first value is performed such that the predetermined
5 number of lines comprises only a single line.
23. The method of claim 15, further comprising:
receiving a master identifier corresponding to the master; and
selecting the prefetch counter from a plurality of prefetch
10 counters based on the master identifier.



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APPL NO.	FILING OR 371 (e) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/631,136	07/31/2003	2186	750	SC12888TH	4	18 23	2 3

CONFIRMATION NO. 3949

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OC000000011859397

Date Mailed: 02/10/2004

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Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 10/28/2003

Projected Publication Date: 02/03/2005

Non-Publication Request: No

Early Publication Request: No

Title

Prefetch control in a data processing system

Received

FEB 16 2004

Motorola Law Dept.